CHUNG-CHENG (ROY) LOU

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http://sites.google.com/site/roylou/ *Permanent Resident*

Ph.D candidate expert in video coding with 2.5 years hardware architect experience. Extensively knowledge of image/video compression and processing, machine learning, and parallel computing.

EDUCATION

University of Southern California, Los Angeles, California
Ph.D., Electrical Engineering, minor in Computer Science, GPA 4.0/4.0 Aug 2007 - May 2011
M.S., Electrical Engineering, GPA 3.92/4.0 2005

National Tsing-Hua University, Hsinchu, Taiwan
B.S., Electrical Engineering, signal processing & computer architecture related GPA 3.83/4.0 2002

Selected Coursework:

- Multimedia System Design
- Multimedia Data Compression
- Analysis of Algorithms
- Operating System
- Computer Vision
- Adaptive Digital Signal Processing
- Computer Architecture
- Mathematical Pattern Recognition
- Random Processes in Engineering

SKILLS

Professional: Image / video coding and processing, machine learning, pattern recognition, multiple-core parallel computing, low power computing, computer vision.
Computer Languages: C, C++, Matlab, Perl, assembly language, JM, FFmpeg, OpenCV.

PROFESSIONAL EXPERIENCE

Research Assistant, *Media Communications Lab, University of Southern Calif., Los Angeles, CA* 2008 - present

- Analyze and research high performance parallel H.264 video codec in multiple core processors.
- Investigate low-power H.264 video codec for mobile applications.

Senior Hardware Architect, *Mobile department, NVIDIA Cooperation, Santa Clara, CA* 2006 - 2008
Hardware Intern, *Mobile department, NVIDIA Cooperation, Santa Clara, CA* 2005

- Developed H.264 / MPEG4 encoder behavior algorithm model for mobile devices.
- Designed and tested H.264 / MPEG4 encoder hardware architecture model (C model), including: B-frame, motion estimation, motion vector predictor calculation, sub-pel interpolation, multiple reference frame, and handling of memory transaction clients.
- Implemented motion compensation by assembly micro-code.
- Developed flexible simulation infrastructure, including command line parser and driver, for hardware verification.

DECT Software Developer, *DBTEL Inc., Taipei, Taiwan* 2004

- Developed user interface and driver level program of Digital Cordless Telephone Technology (DECT).

Research Assistant, *Video Signal Processing Lab, National Tsing-Hua University, Hsinchu, Taiwan* 2001 - 2002

- Designed a real-time video down-sampling algorithm in DCT domain, including transcoding, compression, and transmission.
- Implemented video encoder and decoder with GUI. All of these components were connected via winsock TCP/IP.

SELECTED RESEARCH PROJECTS

3D Display User Interface System, *cooperated with Acer Inc.* Feb 2009 - Mar 2010
Serving as project leader. Designed stereo-vision based gesture recognition and 3D user interaction system without users wearing extra devices. 4 patents pending.

Automatic 3D Stereoscopic Video Format Detection, *cooperated with ETC @ USC* Jun 2009 - Oct 2009
Serving as project leader. Developed real-time low-complexity automated 3D stereoscopic video format detection system.

Adaptive Wind Noise Cancellation, *final project, Adaptive Digital Signal Processing* Jan 2008 - May 2008
Designed adaptive wind noise cancellation algorithm from human voice by Least Mean Square (LMS) method.

Realization of Multimedia Compression, *final project, Multimedia Data Compression* Jan 2005 - May 2005
Implemented various of compression techniques, including Huffman, Lempel-Ziv, Arithmetic, QM, Vector Quantization, Progressive JPEG compression, MPEG-1/2 compression standard with rate control and fast motion search.

Building an OS on Nachos, *final project, Operating Systems and Distributed Systems* Aug 2004 - Dec 2004
Built various of OS features on Nachos OS prototype, including thread synchronization (semaphores, locks, and monitors), multiprogramming, system calls, virtual memory, and distributed systems via remote procedure call (RPC).